REMARKS

Rejections under 35 USC §102(b)

Claims 1, 2 and 6-8 are rejected under 35 USC §102(b) as being anticipated by Nishiguchi (U.S. Patent No. 5,461,261).

Claim 1 recites as follows:

> A method of manufacturing a semiconductor device comprising, **in the recited order**, the steps of:
> [(a)] **forming an insulating film** on a surface of a semiconductor element or a circuit wiring board having electrodes on the surface thereof;
> [(b)] forming openings in the insulating film by patterning the insulating film and then removing portions of the insulating film above the electrodes;
> [(c)] supplying a first metal into the openings;
> [(d)] **heating the first metal to melt and coagulate the first metal**;
> [(f)] supplying a second metal into the openings on the first metal;
> [(g)] **heating the first metal and the second metal to melt and coagulate the first metal and the second metal**; and
> [(h)] **removing the insulating film**.

(Alphabetic order added.) Thus, claim 1 is not claiming a bump including two metal layers in general, but a method with specific steps in the recited order. According to the present invention, the insulating film formed in step (a) is removed in step (h). Also, heating step (d) is inserted between steps (c) and (d).

Nishiguchi discloses a semiconductor device with bumps. According to Nishiguchi, the semiconductor chip is provided with bumps each formed by alternately building up two types of metal materials capable of forming a eutectic alloy. A portion in Nishiguchi, referred by the Examiner reads as follows:

> **According to the mounting method** of the semiconductor chip of the present invention, there are bumps formed by alternately building up the two types of metal materials capable of forming a eutectic alloy, so that the eutectic alloy reaction takes place at each boundary surface between layers. Melting of each boundary surface between layers may fully soften the entire bump.

Here, the eutectic alloy reaction and melting take place when the semiconductor chip is mounted. In contrast, the first metal and the second metal melt and coagulate before the insulating film formed in step (a) is removed in step (h).

Also, Figs. 3-19 and relevant explanations in Nishiguchi do not teach or suggest the steps of claim 1 in the recited order.

For at least these reasons, claim 1 patentably distinguishes over Nishiguchi. Claims 2 and 6-8, depending directly from claim 1, also patentably distinguish over Nishiguchi for at least the same reasons.

Rejections under 35 USC §103(a)

Claims 3-5 are rejected under 35 USC §103(a) as being obvious over Nishiguchi (U.S. Patent No. 5,461,261) in view of Nakata et al. (U.S. Patent Publication No. 2004/0079194).

Nakata et al. has been cited for allegedly disclosing use of Bi in a Sn composition since Bi forms a low melting point alloy phase with Sn. Such disclosure, however, does not remedy the deficiencies of Nishiguchi discussed above.

For at least these reasons, claims 3-5, depending directly or indirectly from claim 1, also patentably distinguish over Nishiguchi.

In view of the aforementioned remarks, Applicants submit that that the claims are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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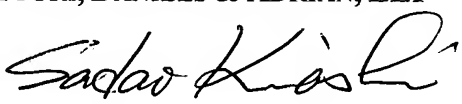

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